PCB Layout and Design Guide for CH7111A

1.0 INTRODUCTION

The discussion and figures presented in this document are based on the 48-pin QFN package of the CH7111A. Chrontel's CH7111A is an innovative, low-power, high performance HDMI re-timing semiconductor device for improving the input TMDS/FRL signal to meet the HDMI 2.1 signal integrity requirement. This device integrates adaptive equalizer, receiver CDR, internal oscillator, high performance PLL and configurable Pre-Emphasis module, and is specially designed targeting for the HDMI 2.1 repeater.

Please refer to the CH7111A datasheet for details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7111A should be placed as close as possible to the respective pins. The following will describe guidelines on how to connect critical pins, as well as the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimal power supply decoupling is accomplished by placing a set of ceramic capacitor at each of the power supply pins. These capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7111A ground pins, in addition to ground vias. Please refer to the attached schematic diagram for details.

2.1.1 Ground Pins

The CH7111A should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7111A ground pins should be connected to its respective decoupling capacitor ground lead directly, and then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to **Table 1** for the Ground pin assignments.

2.1.2 Power Supply Pins

There are some power supply pins: VDD12_RX, VDD12_TX, DVDD, DVD_PLL, VDD_PLL, AVCC_RX, AVCC_TX and AVCC_BG.

Refer to **Table 1** for the Power supply pin assignments. Refer to **Figure 1** for the Power supply reference schematic. Refer to **Figure 2** for Power Supply Decoupling.

Table 1: Power Supply Pin Assignments for the CH7111A (48QFN)

Pin	# of Pins	Type	Symbol	Description
4,7,10,18	4	Power	VDD12_RX	Power Supply (1.2V)
27,33	2	Power	VDD12_TX	Power Supply (1.2V)
20,40	2	Power	DVDD	Power Supply (1.2V)
22	1	Power	DVD_PLL	Power Supply (1.2V)
23	1	Power	VDD_PLL	Power Supply (1.2V)

13	1	Power	AVCC_RX	Power Supply (3.3V)
30	1	Power	AVCC_TX	Power Supply (3.3V)
48	1	Power	AVCC_BG	Power Supply (3.3V)
19,41,Thermal pad	3	Ground	GND	Power Ground

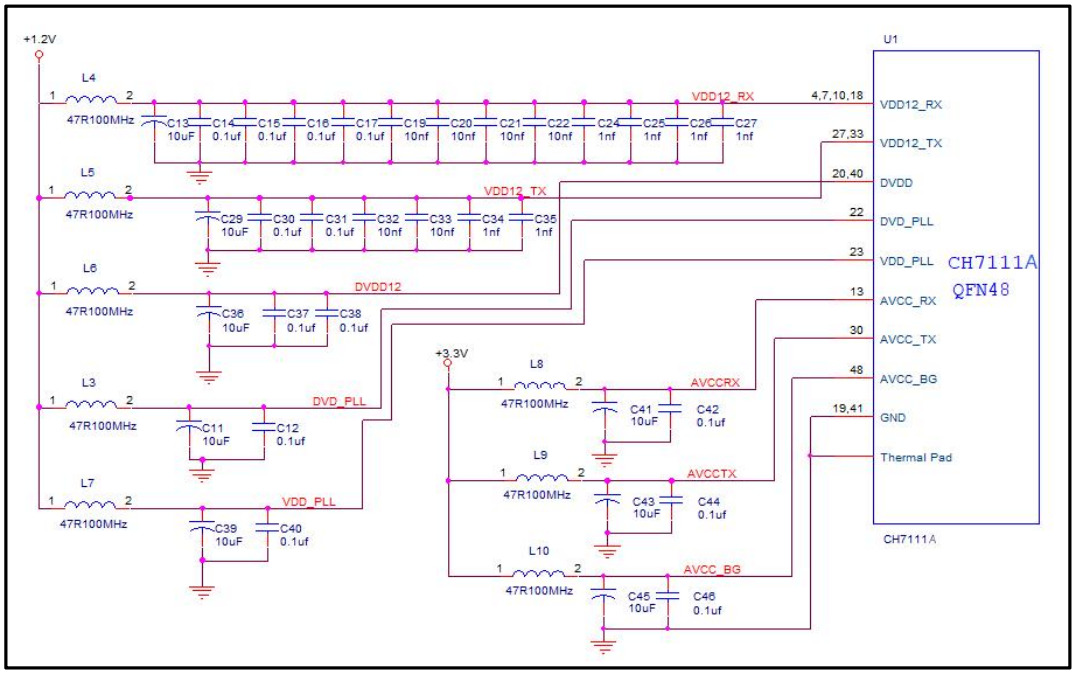

Figure 1 : Power Supply Reference Schematic

2.1.3 Power Sequence

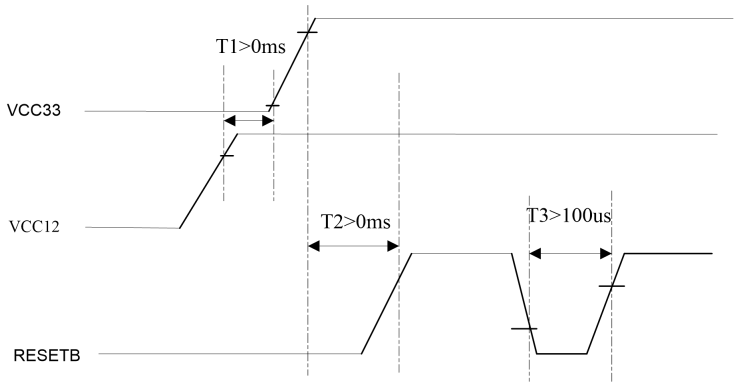

Figure 2 : Power Supply Decoupling and Distribution

Note:

1. **The rising time (10%~90%) of power supply should not exceed 2.5ms.**
2. **The power sequence of VCC12 and VCC33 will not affect the normal functionality.**

To avoid unexpected glitch on during power on, the time from VCC12 up to 90% to VCC33 up to 10%, should be greater than 0ms.

3. **The power supply should be valid (up to 90%) and stable before RESETB becomes invalid.**
4. **The rising threshold of RESETB is AVCC33*0.8. The falling threshold of RESETB is AVCC33*0.2.**
5. **The pulse width of valid RESETB signal should be at least 100us.**
6. **The exposed pad, which is the thermal pad, must be linked to GND.**
7. **All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05Ω at DC; 23Ω at 25MHz & 47Ω at 100MHz. Refer to Fair Rite part #2743019447 for details (an equivalent part can be used for the diagram).**

2.2 Internal Reference Pins

• RBIAS pin

This pin sets the Band-gap Bias Voltage. A 1 KΩ, 1% tolerance resistor should be connected between RBIAS and GND. A 0.1uF capacitor should be connected in parallel with the resistor. Refer to the design example in **Figure 3**.

The distance between the resistor and the CH7111A should be less than 6mm, the shorter and wider trace the better. For optimal performance, this signal should not overlay the analog power or analog output signals.

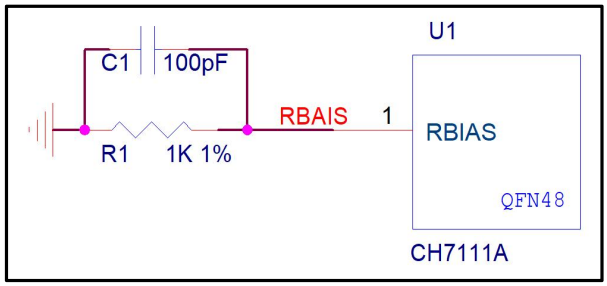

Figure 3 : RBIAS Pin Connection

• LFV

A 1uF capacitor should be connected between LFV and GND. Generally, this capacitor is not connected. Specifically, as shown in **Figure 4**.

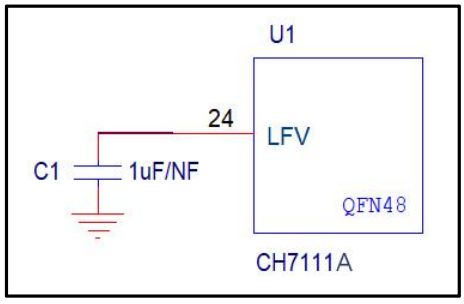

Figure 4 : LFV Pin Connection

• PWR5V

PWR5V is used to monitor the HDMI 5V voltage coming from the HDMI source interface terminal. For those HDMI source ports equipped with HDMI connectors, this pin needs to be connected to the 5V voltage from the connector. For motherboard applications, a 3.3V voltage can be connected to the PWR5V pin through a 10KΩ resistor.

2.3 General Control Pins

• RSTB

RESETB pin is the chip reset pin for the CH7111A. The CH7111A will be reset when this pin is low.

There are two reset methods. One is RC reset. The power supply should be valid and stable before RESETB becomes invalid as shown in **Figure 5**. A 1MΩ and 0.1uF RC reset circuit is recommended.
Another method is using an external reset signal. In this case, the power supply should be valid and stable before the reset signal is valid. The pulse width of valid reset signal should be at least 100us. The timing is shown in **Figure 2.**

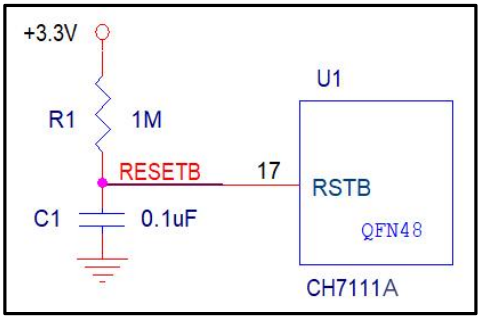

Figure 5 : RBIAS Pin Connection

• GPIO0,GPIO1,GPIO2,GPIO3

General Purpose Input/Output Interface

2.4 Serial Port Control Pins

• SPC and SPD

SPC and SPD function as a serial interface where SPS is the bi-directional data and SPC is an input-only serial clock. In the reference design, SPC and SPD pins are pulled up to +3.3V with 6.8KΩ resistors. The resistors are connected in series with 22pF capacitors to the ground. These two pins need to be pulled to the test points for debugging and updating the firmware. Refer to **Figure 6** for specific details.

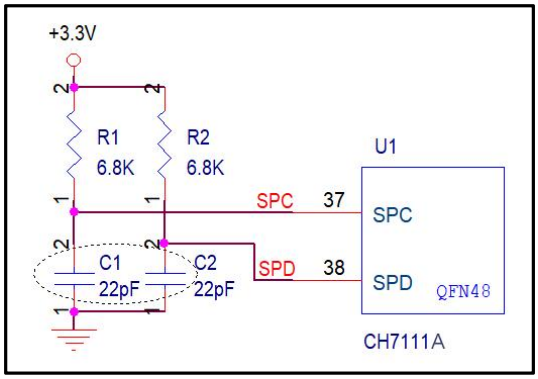

Figure 6 : SPC and SPD Pin Connection

• DDC_SCL_SRC, DDC_SDA_SRC, DDC_SCL_SNK, DDC_SDA_SNK

The DDC_SCL_SRC, DDC_SDA_SRC signal is used for interfacing with the DDC of the HDMI source. These two pins should be connected to HDMI DDC from HDMI source. DDC_SCL_SRC is the DDC serial clock line of the receiving end device. DDC_SDA_SRC is the DDC serial data line of the receiving end device. These two pins are respectively connected to +5V or +3.3V through 10KΩ resistors, it is usually +5V.

The DDC_SCL_SNK, DDC_SDA_SNK signal is used for interfacing with the DDC of the HDMI sink. These two pins should be connected to HDMI DDC from Sink. DDC_SCL_SNK is the DDC serial clock line of the transmitting device. DDC_SDA_SNK is the DDC serial data line of the transmitting device. These two pins are respectively connected to +5V through 1.8KΩ resistors.

CH7111A will configure its internal registers by listening HDMI DDC signals. PIN46 and PIN47 are used to connect to the listening signals. Therefore, these two pins are generally used to connect to HDMI RX DDC signals.

CH7111A has an internal DDC buffer, which can be configured in either passive or active mode. Signals from PIN46 and PIN47 are connected to PIN44 and PIN45 through this DDC buffer. Therefore, PIN44 and PIN45 are generally used to connect HDMI TX DDC signals. Refer to **Figure 7** for specific details.

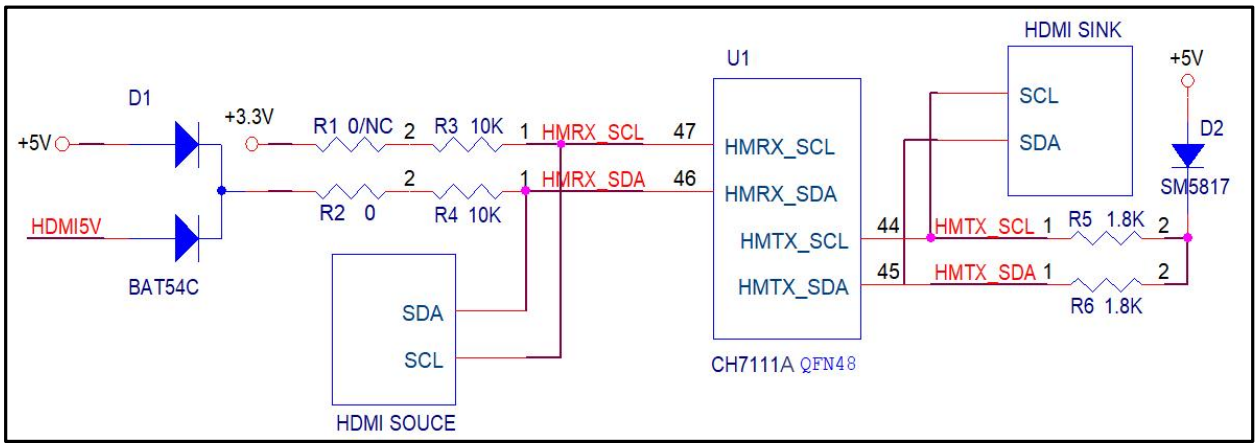

Figure 7 : DDC Through Chip

Customers can also bypass the HDMI RX DDC signal to HDMI TX without using the DDC buffer inside CH7111A. However, the DDC signal must be connected to PIN46 and PIN47. Generally, customers can use resistors to choose whether to bypass CH7111A for DDC signals. Refer to **Figure 8** for specific details.

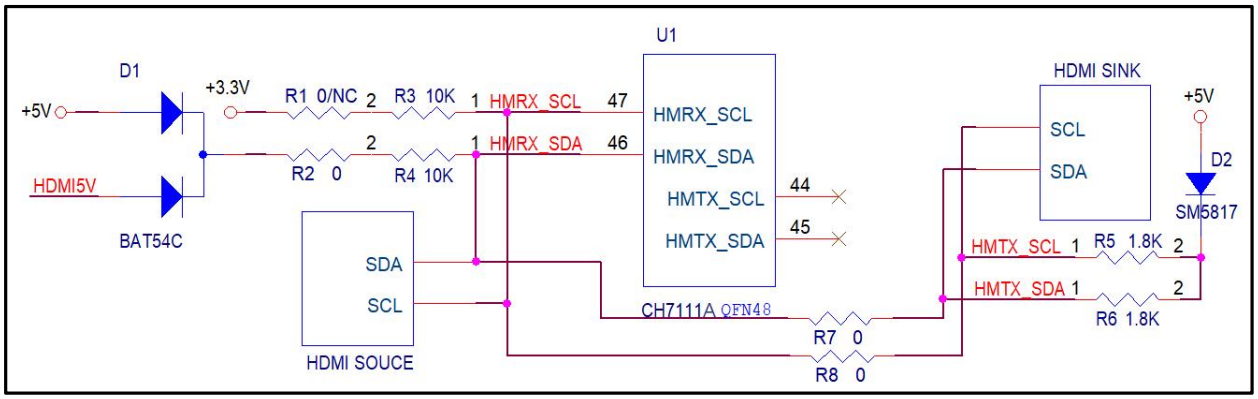

Figure 8 : DDC Bypass

2.5 HDMI RX Port Signal Pins

• RX_CKP/N,RX_D2P/N, RX_D1P/N, RX_D0P/N

Those four pair signals of HDMI RX are high frequency differential pairs, and should be routed by precaution. Please refer to the **section 2.7** for layout guide.

• HPD_OUT

This output pin is connected to GND through a 47KΩ resistor. Refer to the design example in **Figure 9**.

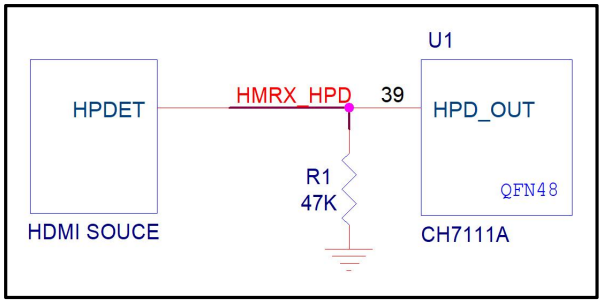

Figure 9 : HPD_OUT Connection

2.6 HDMI TX Port Signal Pins

HDMI output is shown in **Figure 11**.

• TX_CKP/N,TX_D2P/N, TX_D1P/N, TX_D0P/N

Those four pair signals of HDMI TX are high frequency differential pairs, and should be routed by precaution. Please refer to the **section 2.7** for layout guide.

• HPD_IN

This pin is connected to GND through a 47KΩ resistor. Refer to the design example in **Figure 10**.

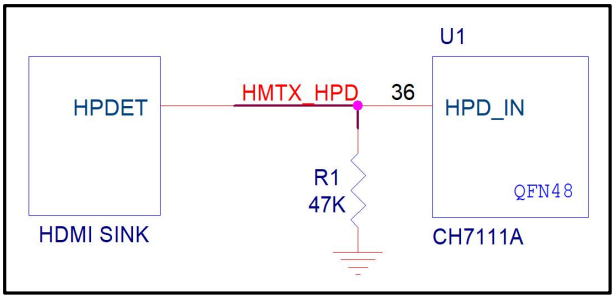

Figure 10 : HPD_IN Connection

2.7 HDMI Differential Trace Layout

2.7.1 Differential Pair Impedance

HDMI signal have four high frequency differential pairs. For HDMI input, those differential pairs are RX_CKP/N, RX_D2P/N, RX_D1P/N, RX_D0P/N. For HDMI output, those differential pairs are TX_CKP/N, TX_D2P/N, TX_D1P/N, TX_D0P/N.

To match the external cable impedance and maintain the maximal energy efficiency it is important that those high frequency differential pairs of HDMI meet the impedance target of 100 Ω ±10% for the differential data/clock traces. The restriction of this impedance target is to prevent any loss of signal strengths resulting from a reflection of unwanted signals. The impedance can be acquired by proper design of trace length, trace width, signal layer thickness, board dielectric, etc.

Since the digital serial data of the CH7111A may be toggled at speeds up to 12Gbps FRL data rate, it is strongly recommended that the connection of these video signals between the graphics controller and the CH7111A be kept as short as possible, avoid discontinuities in the reference plane and be isolated as much as possible from the analog outputs and analog circuitry. For optimal performance, these signals should not overlay the analog power or analog output signals. When a signal pair has to changes layers, the ground stitching vias should be placed close to the signal vias. A minimum of 1 to 3 stitching vias per pair of signals is recommended. Never route a trace so that it straddles a plane split. It is recommended that 5 mils traces be used in routing these signals. There should be 7 mils spacing between each intra pair. The length for a pair of intra differential signals should be matched within 2 mils. The length for inter pairs should be matched within 5mils. The wiring should avoid having a bending angle less than 45 degrees.

Use the smallest size vias and connector pads. It is recommended that 12 mils inner diameter and 18 mils outer diameter vias or smaller one should be used in routing these signals. At most one via can be used on trace.

2.7.2 Trace Routing Length

To prevent from capacitive and impedance loading, trace lengths should be kept as minimal as possible. Vias and bends should always be minimized; inductive effects may be introduced, causing spikes in the signals. Trace routing lengths from CH7111A to the HDMI connector are limited to a maximum of 2 inches. The CH7111A should be as close to the HDMI connector as possible.

2.7.3 Length Matching for Differential Pairs

The HDMI specifies the intra-pair skew and the inter-pair skew as in **Table 2**. The intra-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between the true and complement signals. The inter-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between any two single-ended data signals that do not constitute a differential pair.

Table 2 : Maximum Skews for the HDMI Transmitter

Skew Type	Maxumum at Transmitter
Intra-pair Skew	0.15 T_{bit}
Inter-pair Skew	0.20 T_{pixel}

Where T_{bit} is defined as the reciprocal of Data Transfer Rate and T_{Pixel} is defined as the reciprocal of Clock Rate. Therefore, T_{Pixel} is 10 times T_{bit}. In other words, the intra-pair length matching is much more stringent than the inter-pair length matching.

It is recommended that length matching of both signals of a differential pair be within 2 mils. Length matching should occur on a segment by segment basis. Segments might include the path between vias, resistor pads, capacitor pads, a pin, an edge-finger pad, or any combinations of them, etc. Length matching from one pair to any other should be within 5 mils.

Note that lengths should only be counted to the pins or pad edge. Additional etch within the edge-finger pad, for instance, is electrically considered part of the pad itself.

2.8 ESD Protection for HDMI Interface

In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each HDMI Outputs (data and clock).

International standard EN 55024:1998 establishes 4kV as the common immunity requirement for contact discharges in electronic systems. 8kV is also established as the common immunity requirement for air discharges in electronic systems. International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 establishes the immunity testing and measurement techniques.

System level ESD testing to International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 has confirmed that the proper implementation of Chrontel recommended diode protection circuitry, using ALPGA&OMEGA AOZ8S202UD4 diode array devices, will protect the CH7111A device from HDMI transmitter discharges of greater than 8kV (contact) and 10kV (air). The AOZ8S202UD4 have a typical capacitance of only 0.15pF between I/O pins. This low capacitance won't bring too much bad effect on HDMI eye diagram test.

Figure 11 show the connection of HDMI connectors, including the recommended design of AOZ8S202UD4 diode array devices. HDMI connector is used to connect the CH7111A HDMI outputs.

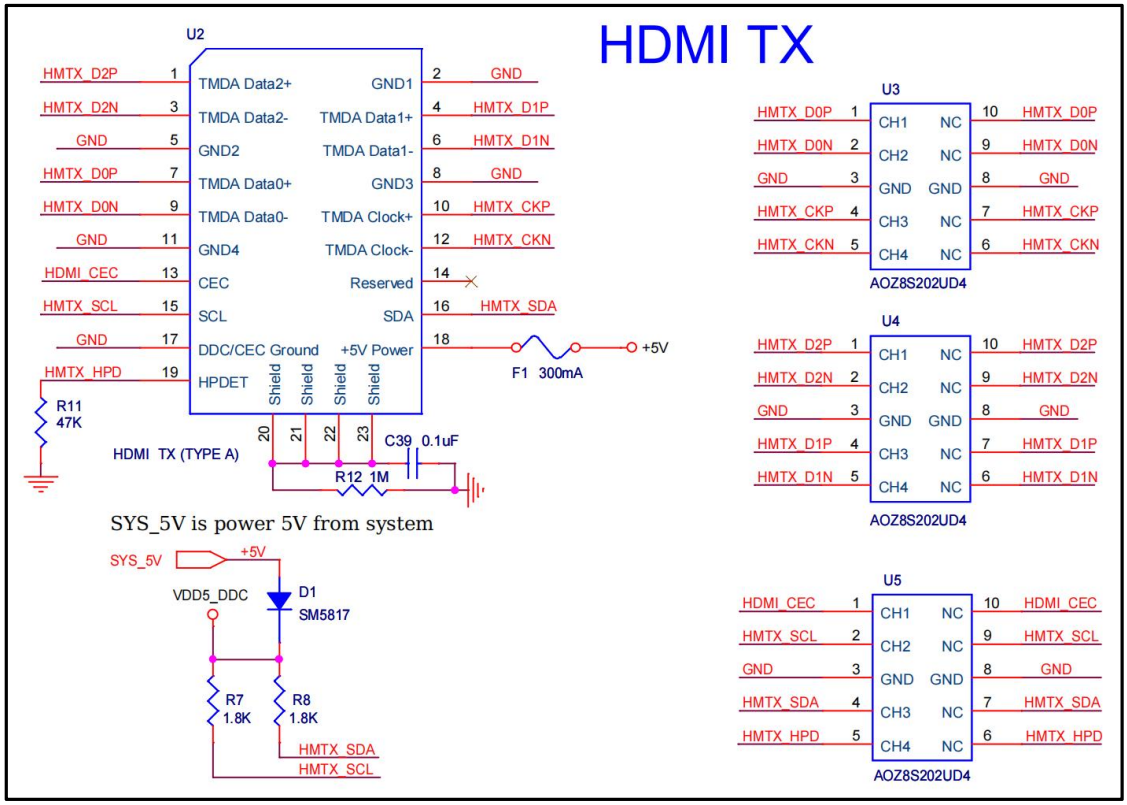

Figure 11 : HDMI Outputs

2.9 Thermal Exposed Pad Package

The CH7111A is available in a 48-pin QFN package with exposed thermal pad. The advantage of the exposed thermal pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed thermal pad package provides a means of reducing the thermal resistance of the CH7111A. Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed thermal pad of the package should be soldered to the PCB as shown in **Figure 12**.

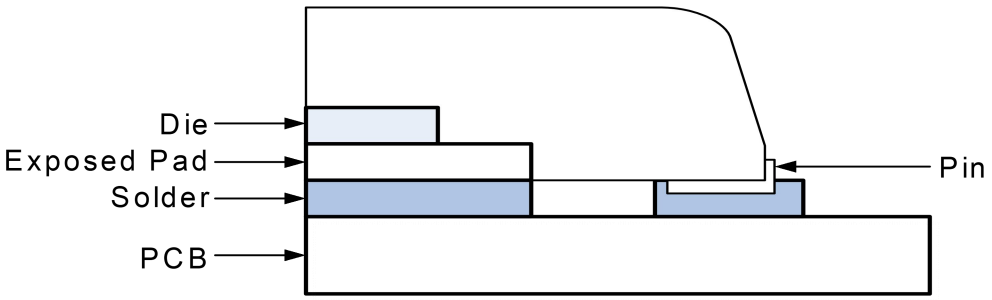

Figure 12: Cross-section of exposed thermal pad package

3.0 REFERENCE DESIGN EXAMPLE

The following schematics are to be used as a CH7111A PCB design example only. It is not a complete design. Those who are seriously doing an application design with CH7111A and would like to have a complete reference design schematic should contact Chrontel Applications group for further support, Inc.

3.1 Schematic of Reference Design Example

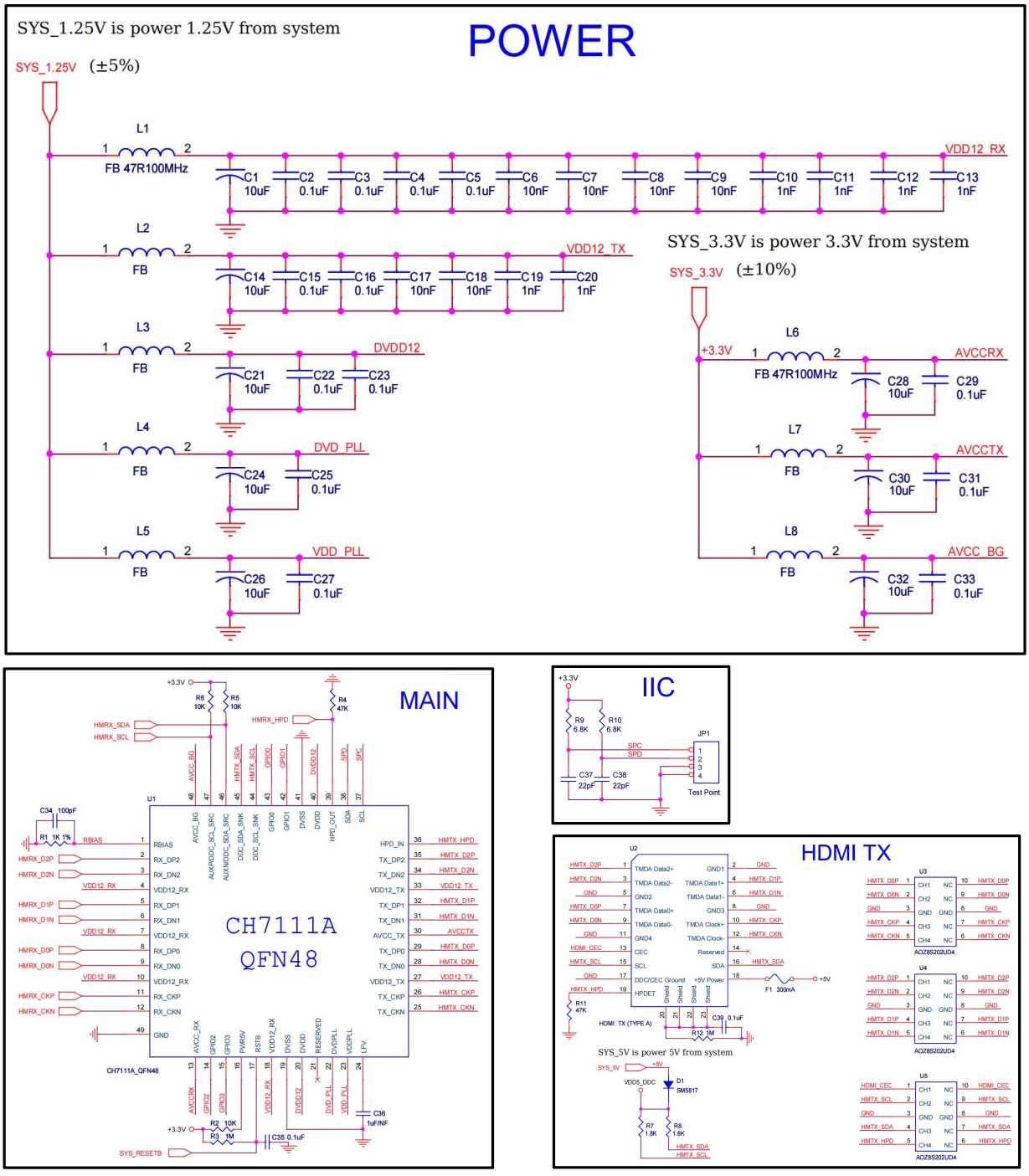

Figure 13: HDMI Reference Schematic

4.0 REVISION HISTORY

Table 3: Revisions

Rev. #	Date	Section	Description
0.1	06/10/2026	All	Layout Guide and Design Guide for CH7111A release.

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